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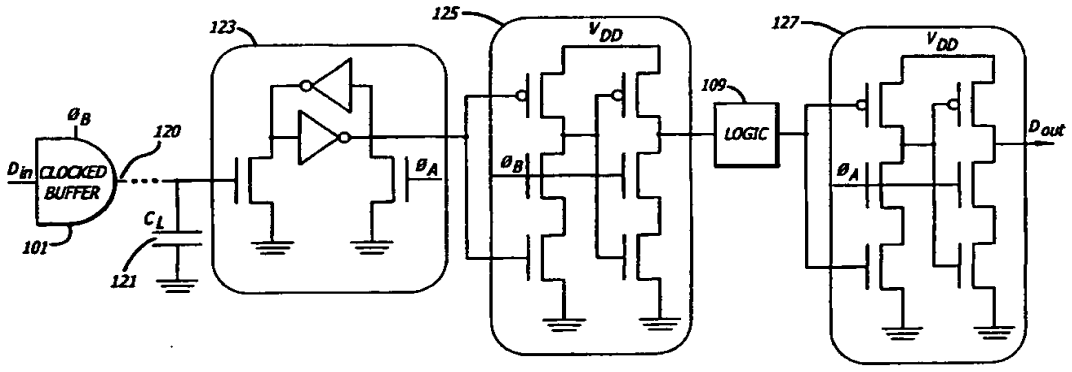
(54) Title: HIGH-PERFORMANCE CLOCK-POWERED LOGIC



(57) Abstract: High performance clock-powered logic runs at below supply levels and reduces the need for faster digital logic circuitry. In a preferred embodiment, a clocked buffer (101) is used to drive the signal line. The receiving end of the line is connected to a jam latch (123), preferably followed by an n-latch (125), followed by the digital logic (109), and followed by a second n-latch (127). The first n-latch is eliminated in an alternative embodiment, preferably one that uses complementary data signals.

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